WHAT IS CLAIMED IS:

1. A method of adjusting a phase of a dot clock signal for a video signal, said method comprising the steps of:

(a) sampling said video signal by a plurality of dot clock signals that are expected to have different phase relationships to said video signal, thereby obtaining plural sets of image data;

(b) carrying out a prescribed operation for each set of image data to obtain a phase-related index representing the phase relationship of said each set of image data, and determining a desirable phase for said dot clock signal based on said phase-related indexes of said plural sets of image data; and

(c) applying an optimum delay to said dot clock signal to have the desirable phase.

2. A method in accordance with claim 1, wherein

said step (a) comprises the step of:

applying a plurality of different delays to a reference clock to generate said plurality of dot clock signals, and sampling said video signal by each dot clock signal to obtain said plural sets of image data respectively representing images at an identical position on a screen; and wherein

said step (b) comprises the steps of:

(1) calculating values of a function representing sharpness of said plural sets of image data as said phase-related indexes corresponding to said plurality of delays;

(2) determining an extreme of said values of said function against said plurality of delays; and

(3) selecting a delay among said plurality of delays as the optimum delay to attain the desirable phase, said selected delay corresponding to the extreme of said values of said function.

3. A method in accordance with claim 2, wherein said plurality of delays are in a range corresponding to a phase of at least 2π.

4. A method in accordance with claim 2, wherein said plurality of delays have a constant delay step.

5. A method in accordance with claim 2. further comprising the step of: executing said calculating a value of said function and said determining an extreme of said values of said function each time one of said plurality of delays is selected to be applied, and terminating a process of said steps (a) through (c) when the extreme of said values of said function is obtained.

6. A method in accordance with claim 1, wherein said step (a) comprises the steps of:

multiplying a frequency of a horizontal synchronizing signal of said video signal by a first factor to generate a first dot clock signal, said first factor being different from an appropriate second factor that is to be used for multiplying the frequency of said horizontal synchronizing signal to generate said dot clock signal having the desirable phase, said first dot signal including a plurality of signal phases which can be considered as said plurality of dot signals; and

sampling said video signal by said first dot clock signal to obtain first image data on a specific line of the screen; and wherein

said step (b) comprises the steps of:

dividing said first image data into a plurality of first image data blocks;

calculating values of said function representing sharpness of said plurality of first image data blocks as said phase-related indexes of said plurality of first image data blocks, respectively;

determining the extreme of said values of said function with respect

to said plurality of first image data blocks; and

selecting a delay corresponding to a specific first image data block related to the extreme of said values of said function as the optimum delay to attain the desirable phase.

7. A method in accordance with claim 6, wherein the delay corresponding to said specific first image data block related to the extreme of said values of said function is determined based on the difference between said first and second factors and on a position of said specific first image data block in said plurality of first image data blocks.

8. A method in accordance with claim 6, wherein

said optimum delay can be adjusted by a predetermined delay step in said step (c); and

said step (b) comprises the step of: dividing said first image data over an entirety of said specific line by a divisional number into said plurality of first image data blocks, said divisional number being equal to an integral multiple of a quotient obtained by dividing a difference between said first and second factors by a product of a frequency of said first dot clock signal and the delay step.

9. A method in accordance with claim 6, wherein an absolute value of the difference between said first and second factors is equal to two.

10. A method in accordance with claim 6, wherein said step (a) further comprises the steps of:

multiplying the frequency of said horizontal synchronizing signal of said video signal by said second factor to generate a second dot clock signal; and

sampling said video signal by said second dot clock signal to obtain

second image data on the specific line of the screen; and wherein

said step (b) further comprises the steps of:

dividing said second image data into a plurality of second image data blocks in the same manner as the division of said first image data;

calculating values of said function representing sharpness of said plurality of second image data blocks; and

dividing said values of said function for said plurality of first image data blocks by said values of said function for said plurality of second image data blocks, respectively, and setting respective quotients obtained by said dividing as said phase-related indexes corresponding to said plurality of first image data blocks.

11. A method in accordance with claim 10, wherein said step (b) further comprises the step of:

when said plurality of first image data blocks includes a block whose value of said function is less than a threshold value, carrying out an interpolation on the value of said function for said block with respect to said plurality of first image data blocks and said plurality of second image data blocks prior to said dividing said values of said function.

12. A method in accordance with claim 2, wherein said function is an unequivocal and monotone function with respect to a sum of squared differences between image data values at adjoining pixel positions.

13. a method in accordance with claim 12, wherein said function is a sum of absolute values of the differences between image data values at adjoining pixel positions.

14. A method in accordance with claim 2, wherein said function is an unequivocal and monotone function with respect to a statistical variance of

said image data.

15. A method in accordance with claim 2, wherein said step of determining an extreme of the values comprises the steps of:

carrying out a filtering process with a low-pass filter on one dimensional array of said values of said function; and

determining the extreme from one-dimensional array of processed values of said function obtained by said filtering process.

16. An apparatus for adjusting a phase of a dot clock signal for a video signal, said apparatus comprising:

sampling means for sampling said video signal by a plurality of dot clock signals that are expected to have different phase relationships to said video signal, thereby obtaining plural sets of image data;

phase determining means for carrying out a prescribed operation for each set of image data to obtain a phase-related index representing the phase relationship of said each set of image data, and determining a desirable phase for said dot clock signal based on said phase-related indexes of said plural sets of image data; and

delay setting means for applying an optimum delay to said dot clock signal to have the desirable phase.

17. A method of adjusting a frequency of a dot clock signal for a video signal, said method comprising the steps of:

(a) multiplying a frequency of a horizontal synchronizing signal of said video signal by a first factor to generate a first dot clock signal;

(b) sampling said video signal by said first dot clock signal to obtain image data;

(c) analyzing said image data to determine a first value representing a length of an effective signal area on one line of said image data;

(d) carrying out an operation using said first value representing the length of said effective signal area and a known second value representing a true length of said effective signal area, thereby determining a desirable second factor; and

(e) multiplying the frequency of said horizontal synchronizing signal by said second factor to generate a desirable second dot clock signal.

18. A method in accordance with claim 17, wherein said step (c) comprises the steps of:

determining a starting position and a terminal position of said effective signal area; and

calculating said first value representing the length of said effective signal area from a difference between said starting position and said terminal position.

19. A method in accordance with claim 18, wherein said step of determining said starting position and said terminal position comprises the step of:

detecting variation points having a remarkable level change of said image data as said starting position and said terminal position.

20. A method in accordance with claim 19, wherein said step of detecting variation points as said starting position and said terminal position comprises the step of: selecting points at which a difference between image data values at adjoining pixels on said one line of image data exceeds a threshold value, as said variation points.

21. A method in accordance with claim 18, further comprising the step of:

calculating a second starting position of said effective signal area for

second image data obtained by said second dot clock signal, on the basis of said starting position of said effective signal area for said image data obtained by said first dot clock signal.

22. A method in accordance with claim 17, wherein said operation carried out in said step (d) includes multiplication of said first factor by a ratio of said second value to said first value representing the length of said effective signal area.

23. A method in accordance with claim 22, wherein said operation carried out in said step (d) further includes a rounding operation for rounding the result of said multiplication.

24. A method in accordance with claim 17, wherein said step (c) comprises the step of:

obtaining a maximum value for each identical position on each line over plural lines of said image data, and using image data consisting of said maximum values as a target of said analyzing.

25. A method in accordance with claim 17, wherein said step (b) comprises the step of: obtaining said image data for a specific range including the starting position and the terminal position of said effective signal area but does not include the entirety of said one line.

26. An apparatus for adjusting a frequency of a dot clock signal for a video signal, said apparatus comprising:

dot clock generation means for multiplying a frequency of a horizontal synchronizing signal of said video signal by a first factor to generate a first dot clock signal;

sampling means for sampling said video signal by said first dot clock

signal to obtain image data;

first operation means for analyzing said image data to determine a first value representing a length of an effective signal area on one line of said image data;

second operation means for carrying out an operation using said first value representing the length of said effective signal area and a known second value representing a true length of said effective signal area, thereby determining a desirable second factor; and

factor setting unit for setting said desirable second factor in said dot clock generation means and thereby enabling said dot clock generation means to multiply the frequency of said horizontal synchronizing signal by said second factor to generate a desirable second dot clock signal.

27. A method of adjusting a frequency of a dot clock signal for a video signal, said method comprising the steps of:

(a) multiplying a frequency of a horizontal synchronizing signal of said video signal by a first factor to generate a first dot clock signal;

(b) sampling said video signal by said first dot clock signal to obtain image data;

(c) obtaining a number of beats over one line of said image data;

(d) correcting said first factor with said number of beats, thereby obtaining a desirable second factor; and

(e) multiplying the frequency of said horizontal synchronizing signal by said second factor to generate a second dot clock signal that can be used to sample image data without beats.

28. A method in accordance with claim 27, wherein said step (c) comprises the steps of:

(i) transforming said image data to transformed image data using a symmetrical monotone transformation function that has a symmetrical

output level with respect to a predetermined input level; and

(ii) determining said number of beats based on said transformed image data.

29. A method in accordance with claim 28, wherein said transformation function is non-linear on both sides of said predetermined input level.

30. A method in accordance with claim 29, wherein said transformation function is a quadratic function.

31. A method in accordance with claim 28, wherein said step (i) comprises the step of:

carrying out a filtering process with a high-pass filter prior to said transformation with said transformation function; and wherein

said step (ii) comprises the step of:

carrying out a filtering process with a low-pass filter for said transformed image data prior to said determination of said number of beats.

32. A method in accordance with claim 28, wherein said step (ii) comprises the step of:

carrying out a frequency analysis on said transformed image data to determine said number of beats.

33. A method in accordance with claim 32, wherein said step of carrying out frequency analysis comprises the step of carrying out fast Fourier transform of said transformed image data to determine a frequency of said beats.

34. A method in accordance with claim 32, wherein said step of

carrying out frequency analysis comprises the step of: processing said transformed image data with a plurality of comb filters, and determining a frequency of said beats based on a frequency passing through said plurality of comb filters.

35. A method in accordance with claim 27, wherein said step (b) comprises the step of obtaining first image data and second image data by two kinds of said first dot clock signal having a first phase and a second phase that are different from each other; and wherein

said step (c) comprising the step of carrying out a correlation analysis on said first image data and said second image data to determine said number of beats.

36. A method in accordance with claim 35, wherein the difference between said first phase and said second phase is about half a cycle of said first dot clock signal.

37. A method in accordance with claim 35, wherein said step of carrying out correlation analysis comprises the steps of:

(i) allocating a first value to pixel positions having a relatively large difference between said first image data and said second image data while allocating a second value to pixel positions having a relatively small difference between said first image data and said second image data, thereby generating binary data consisting of said first value and said second value; and

(ii) processing said binary data to determine said number of beats.

38. A method in accordance with claim 37, wherein said step (i) comprises the step of:

generating at least one of first binary data, second binary data, and

third binary data, wherein

said first binary data is to be generated by allocating said first value to pixel positions having a relatively large difference between said first image data and forward-shifted second image data obtained by shifting a pixel position of said second image data forward by one pixel and by allocating said second value to pixel positions having a relatively small difference between said first image data and said forward-shifted second image data;

said second binary data is to be generated by allocating said first value to pixel positions having a relatively large difference between said first image data and said second image data and allocating said second value to pixel positions having a relatively small difference between said first image data and said second image data; and

said third binary data being to be generated by allocating said first value to pixel positions having a relatively large difference between said first image data and backward-shifted second image data obtained by shifting a pixel position of said second image data backward by one pixel, and by allocating said second value to pixel positions having a relatively small difference between said first image data and said backward-shifted second image data; and wherein

said step (ii) comprises the step of determining said number of beats using at least one of said first through third binary data.

39. A method in accordance with claim 38, wherein said step (ii) comprises the steps of:

providing a first pair of binary data including said first and second binary data and a second pair of binary data including said second and third binary data;

executing a toggle operation, with respect to each of said first and second pairs of binary data, using a rise of one binary data of each pair and a rise of the other of each pair to generate two toggled binary data for said first

and second pairs of binary data;

selecting one of said two toggled binary data which has an average closer to 0.5: and

measuring a number of pulses included in one line of said selected toggled binary data, thereby determining said number of beats.

40. A method in accordance with claim 39, wherein said step of measuring a number of pulses comprises the step of obtaining a mean distance between variation points of said selected toggled binary data and calculating said number of pulses from said mean distance.

41. A method in accordance with claim 38, wherein said step (ii) comprises the steps of:

selecting at least one of said first through third binary data, and deleting an interval between a rise and a fall of said selected binary data that is less than a predetermined value, thereby generating modified binary data

selecting at lease one modified binary data which has an average close to 0.5; and

measuring a number of pulses included in one line of said selected modified binary data, thereby determining said number of beats.

42. A method in accordance with claim 41, wherein said operation of generating said modified binary data comprises the step of:

carrying out a one-dimensional expansion process on one line of said selected binary data, for expanding one of said first and second values by a predetermined width; and

carrying out a one-dimensional contraction process on said binary data after said one-dimensional expansion process, for contracting said one of said first and seconds value by said predetermined width.

43. A method in accordance with claim 41, wherein said step of measuring a number of pulses comprises the step of computing a mean distance between variation points of said modified binary data and calculating said number of pulses from said mean distance.

44. A method in accordance with claim 37, wherein said operation of generating said binary data is implemented by binary-coding two image data used in generating said binary data, respectively, and by obtaining an exclusive OR of the two binary-coded image data.

45. A method in accordance with claim 37, wherein said operation of generating said binary data is implemented by obtaining a difference between two image data used in generating said binary data, and by binary-coding said difference with a predetermined threshold value.

46. An apparatus for adjusting a frequency of a dot clock signal for a video signal, comprising:

dot clock generation means for multiplying a frequency of a horizontal synchronizing signal of said video signal by a first factor to generate a first dot clock signal;

sampling means for sampling said video signal by said first dot clock signal to obtain image data;

first operation means for obtaining a number of beats over one line of said image data;

second operation means for correcting said first factor with said number of beats, thereby obtaining a desirable second factor; and

factor setting means for setting said second factor in said dot clock generation means and thereby enabling said dot clock generation means to multiply the frequency of said horizontal synchronizing signal by said second

factor to generate a second dot clock signal that can be used to sample image data without beats.

47. A dot clock regeneration circuit for regenerating a dot clock signal to be supplied to a sampling circuit for sampling a video signal, said dot clock regeneration circuit comprising:

a PLL circuit for multiplying a frequency of a horizontal synchronizing signal of said video signal by a predetermined factor to generate a reference clock signal;

a delay circuit for delaying said reference clock signal by a predetermined time to generate said dot clock signal;

memory means for storing at least one line of image data supplied from said sampling circuit; and

delay time setting means for controlling a writing process of said image data into said memory means, reading one line of said image data stored in said memory means to carry out a prescribed operation, and setting a delay time in said delay circuit based on the result of said prescribed operation to attain a desirable phase relationship between said video signal and said dot clock signal.

48. A dot clock regeneration circuit in accordance with claim 47, wherein said delay time setting means repeats a procedure of reading one line of said image data stored in said memory means and carrying out said prescribed operation every time when the delay time set in said delay circuit is changed, and determines an optimum delay time to give an optimum phase to said dot clock signal based on the result of said prescribed operation.

49. A dot clock regeneration circuit in accordance with claim 47, further comprising:

addition means for increasing or decreasing said predetermined factor by a preset value to give an offset,

wherein said delay time setting means carries out said prescribed operation for each value of the increased or decreased factor.

50. A dot clock regeneration circuit in accordance with claim 49, wherein said delay time setting means comprises:

means for carrying out said prescribed operation on first image data and second image data to determine an optimum delay time to give an optimum phase to said dot clock signal, said first image data being obtained on the basis of a first factor set in said PLL circuit by said addition means, said second image data being obtained on the basis of a second factor set in said PLL circuit.

51. A dot clock regeneration circuit in accordance with claim 50, wherein said delay time setting means comprises:

means for carrying out an interpolating operation on said first image data and said second image data with respect to a pixel position which has an image data value no more than a specified level in said first image data,.

52. A dot clock regeneration circuit in accordance with claim 51, wherein said prescribed operation is carried out on a plurality of blocks which is divided from said one line of image data by a divisional number, said divisional number being equal to an integral multiple of a quotient obtained by dividing a difference between said first factor and said second factor by the product of a frequency of said dot clock signal and a delay step in said delay circuit.

53. A dot clock regeneration circuit in accordance with claim 50, wherein an absolute value of a difference between said first and second

factors is equal to two.

54. A dot clock regeneration circuit in accordance with claim 47, wherein said prescribed operation includes calculating a squared difference between said image data at adjoining pixel positions read out of said memory means.

55. A dot clock regeneration circuit in accordance with claim 47, wherein said prescribed operation includes calculating an absolute value of a difference between said image data at adjoining pixel positions read out of said memory means.

56. A video signal display apparatus comprising:

sampling means for sampling a video signal;

clock generation means for multiplying a horizontal synchronizing signal by a predetermined frequency division factor to generate a dot clock;

driving means for processing an output of said sampling means;

a display device for displaying an image in response to an output of said driving means;

display timing means for controlling a display timing of said display device;

memory means for storing one line of data output from said sampling means;

write timing means for outputting a write enable signal to said memory means; and

control means for outputting a write arm signal to said write timing means to cause said memory means to store data of a specific line, reading out said data of the specific line stored in said memory means, carrying out a prescribed operation, and setting a factor in said clock generation means based on the result of said prescribed operation.

57. A video signal display apparatus in accordance with claim 56, wherein said memory means has a storage capacity of not greater than a number of pixels of said display device in a horizontal direction.

58. A method of regenerating a dot clock in a video signal display apparatus, said video signal display apparatus comprising: sampling means for sampling a video signal; clock generation means including a PLL circuit for multiplying a horizontal synchronizing signal by a predetermined frequency division factor to generate a dot clock; driving means for processing an output of said sampling means; a display device for displaying an image in response to an output of said driving means; display timing means for controlling a display timing of said display device; memory means for storing one line of data output from said sampling means; write timing means for outputting a write enable signal to said memory means; and control means for outputting a write arm signal to said write timing means to cause said memory means to store data of a specific line, reading out said data of the specific line stored in said memory means, carrying out a prescribed operation, and setting a factor in said clock generation means based on the result of said prescribed operation, said method comprising the steps of:

setting a provisional factor in said PLL circuit and storing data into said memory means;

comparing a difference between said data read out of said memory means at adjoining addresses with a predetermined threshold value to determine a starting address and a terminal address of an effective signal area of said video signal stored in said memory means;

determining a number of dot clocks corresponding to one line of said video signal from a difference between said starting address and said terminal address and said provisional factor; and

setting said number of dot clocks as the frequency division factor in said clock generation means.

59. A method in accordance with claim 58, further comprising the steps of:

repeating a procedure of writing data into said memory means and subsequently reading out said data from said memory means for a plurality of lines of said video signal; and

determining said starting address and said terminal address of said effective signal area based on maximum values at respective addresses in said memory means.

60. A method in accordance with claims 58, further comprising the steps of:

calculating an optimum horizontal display position on a screen displayed on said display device from said starting address of said effective signal area and said factor obtained from the result of said operation, and setting said optimum horizontal display position in said display timing means.

61. A method of regenerating a dot clock in a video signal display apparatus, said video signal display apparatus comprising: sampling means for sampling a video signal; clock generation means for multiplying a horizontal synchronizing signal by a predetermined frequency division factor to generate a dot clock; driving means for processing an output of said sampling means; a display device for displaying an image in response to an output of said driving means; display timing means for controlling a display timing of said display device; memory means for storing one line of data output from said sampling means; write timing means for outputting a write enable signal to said memory means; and control means for outputting a

write arm signal to said write timing means to cause said memory means to store data of a specific line, reading out said data of the specific line stored in said memory means, carrying out a prescribed operation, and setting a factor in said clock generation means based on the result of said prescribed operation, said method comprising the steps of:

processing said data read out from said memory means with a high-pass filter;

carrying out a non-linear operation and subsequently performing fast Fourier transform on the data after the high-pass filter processing;

obtaining a peak in the result of said fast Fourier transform to determine a frequency of a beat component; and

setting a factor in said clock generation means so that a frequency of said beat component becomes equal to zero.

62. A method of regenerating a dot clock in a video signal display apparatus, said video signal display apparatus comprising: sampling means for sampling a video signal; clock generation means for multiplying a horizontal synchronizing signal by a predetermined frequency division value to generate a dot clock; driving means for processing an output of said sampling means; a display device for displaying an image in response to an output of said driving means; display timing means for controlling a display timing of said display device; memory means for storing one line of data output from said sampling means; write timing means for outputting a write enable signal to said memory means; and control means for outputting a write arm signal to said write timing means to cause said memory means to store data of a specific line, reading out said data of the specific line stored in said memory means, carrying out a prescribed operation, and setting a factor in said clock generation means based on the result of said prescribed operation, said method comprising the steps of:

processing the data read out from said memory means with a high-

pass filter;

carrying out a non-linear operation on the data after said high-pass filter processing and subsequently performing an operation with a plurality of comb filters;

determining a frequency of a beat component based on a combination of integral values of the result of said operation with said plurality of comb filters; and

setting a factor in said clock generation means so that a frequency of said beat component becomes equal to zero.

63. A method in accordance with claim 61, wherein said non-linear operation is a squaring operation.

64. A method of regenerating a dot clock in a video signal display apparatus, said video signal display apparatus comprising a PLL circuit for multiplying a horizontal synchronizing signal by a predetermined frequency division factor to generate a dot clock; phase control means for regulating a phase of said dot clock; driving means for processing an output of said sampling means; a display device for displaying an image in response to an output of said driving means; display timing means for controlling a display timing of said display device; memory means for storing one line of data output from said sampling means; write timing means for outputting a write enable signal to said memory means; and control means for outputting a write arm signal to said write timing means to cause said memory means to store data of a specific line, reading out said data of the specific line stored in said memory means, carrying out a prescribed operation, and setting a factor in said clock generation means based on the result of said prescribed operation, said method comprising the steps of:

setting a provisional factor in said PLL circuit, writing data into said memory means, and subsequently reading out first data from said memory

means;

changing a phase control value in said phase control means, writing data into said memory means, and subsequently reading out second data from said memory means;

carrying out a correlation analysis on said fist data and said second data;

carrying out a factor determining operation for determining a total number of pixels corresponding to one line of said video signal based on the result of said correlation analysis; and

setting said total number of pixels as the frequency division factor in said clock generation means.

65. A method in accordance with claim 64, wherein said correlation analysis includes calculating an exclusive OR of third data and fourth data to generate fifth data, said third data being obtained by binary-coding said first data, said fourth data being obtained by binary-coding said second data.

66. A method in accordance with claim 64, wherein said correlation analysis includes calculating a difference between said first data and said second data to generate third data, and binary-coding said third data to generate fourth data.

67. A method in accordance with claim 64, wherein said factor determining operation is executed by the steps of:

calculating a mean distance between adjoining variation points of the resulting data of said correlation operation;

dividing said provisional factor set in said PLL circuit by twice the mean distance and rounding the result of said division to determine a number of beats included in said one line; and

calculating the total number of pixels corresponding to said one line

from either of a sum of and a difference between said provisional factor set in said PLL circuit and said number of beats.

68. A method in accordance with claim 65, wherein said correlation analysis of said first data and said second data is executed by the steps of:

carrying out a first operation in which said second data whose address is less than an address of said first data by one is used, a second operation in which said second data whose address is equal to the address of said first data is used, and a third operation in which said second data whose address is greater than the address of said first data by one is used;

inverting a virtual register based on variation points of the result of said first operation and the result of said second operation to generate said third data;

inverting another virtual register based on variation points of the result of said second operation and the result of said third operation to generate said fourth data;

selecting one of said third and fourth data which has a mean value closer to half a maximum of said third data and said fourth data, as fifth data; and wherein

said factor determining operation includes calculating the total number of pixels corresponding to said one line of said video signal from a mean distance between variation points of said fifth data and said provisional factor set in said PLL circuit.